REMARKS

In the Office Action dated May 20, 2004, the Examiner rejected claims 1, 2, 4, 10-13, 17, and 18 under 35 U.S.C. § 102(b) and rejected claims 3, 5-9, and 14-16 under 35 U.S.C. § 103(a). Claims 1, 8, 13, and 17 have been amended. No new matter has been added. Additionally, claim 12 has been canceled. Applicants respectfully traverse the claim rejections and request reconsideration.

A. Response to the 35 U.S.C. § 102(b) Rejections

Claims 1, 2, 4, 10-13, 17, and 18 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,834,339 ("Distefano"). In amended claim 1, Applicants recite a system for three-dimensional packaging of platelets. The system includes a slotted file and a plurality of platelets that fit into the slotted file. Each of the platelets includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier. The platelets are stacked in the slotted file forming a three-dimensional integrated circuit package. As a result, a three-dimensional integrated circuit package may be formed that provides a very tight spacing tolerance between platelets and that minimizes damage to the platelets during the stacking process.

In contrast, Distefano describes a temporary system for stacking assembled frames to facilitate the removal of voids and gas bubbles within an encapsulant used in attaching and packaging microelectronic devices. The assembled frames include a plurality of chips attached to a substrate that includes a sacrificial substrate. (See, e.g., Distefano, column 9, lines 42-45.) A layer of sheet-like material is attached to the terminal side of the substrate so that the encapsulant does not escape through bonding windows, which could contaminate the

terminals and impede any subsequent electrical connection of the terminals to bond pads. (See, e.g., Distefano, column 9, line 62 to column 10, line 1.) After the encapsulant is cured, the fully encapsulated semiconductor chip packages within the assembled frames are separated from their respective frame/substrate into single packaged chips. (See, e.g., Distefano, column 10, lines 32-35.) Leads can then be detached from the sacrificial substrate and bonded to respective chip contacts. (See, e.g., Distefano, column 10, lines 63-65.)

Distefano describes stacking assembled frames to facilitate mass production of finished parts. (See, e.g., Distefano, column 9, lines 39-42.) Once the encapsulation process is completed, the semiconductor chip packages are removed from the frame assembly and separated. Once separated, the semiconductor chip packages are then connected to the respective chip contacts. Thus, Distefano teaches away from semiconductor chip packages contacting a plurality of electrodes while in the frame assembly and stacking the semiconductor chips into a three-dimensional integrated circuit package.

Distefano's purpose for stacking assembled frames requires only temporary stacking. Locating a plurality of electrodes in the frame assembly or stacking the semiconductor chips into a three-dimensional integrated circuit package is unnecessary for the temporary stacking of assembled frames as described by Distefano. Because Distefano does not show or suggest placing a semiconductor chip into a chip carrier so that the semiconductor chip contacts a plurality of electrodes in the chip carrier or stacking platelets in a slotted file to form a three-dimensional integrated circuit package, Distefano does not show or suggest each and every element of claim 1. Accordingly, Applicants submit that Distefano does not

anticipate claim 1.

Claims 2, 4, 10-13, 17, and 18 depend from claim 1. Accordingly, Applicants also submit that Distefano does not anticipate claims 2, 4, 10-13, 17, and 18 for at least the reasons set forth above.

In light of the above, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 102(b).

B. Response to the 35 U.S.C. § 103(a) Rejections

Claims 3 and 5-9 were rejected under 35 U.S.C. § 103(a) as being obvious in light of Distefano in view of U.S. Patent No. 6,457,515 ("Vafai"). Claims 3 and 5-9 depend from claim 1.

As described above, Distefano does not show or suggest placing a semiconductor chip into a chip carrier so that the semiconductor chip contacts a plurality of electrodes in the chip carrier or stacking platelets in a slotted file to form a three-dimensional integrated circuit package. Vafai is cited for teaching the use of silicon as a heat sink material. (See, Office Action, page 6.) This teaching in Vafai fails to overcome the deficiencies in Distefano. Accordingly, Applicants submit that claims 3 and 5-9 are not obvious in light of the combination of Distefano and Vafai for at least the reasons set forth above.

Claims 14-16 were rejected under 35 U.S.C. § 103(a) as being obvious in light of Distefano in view of U.S. Patent No. 5,140,405 ("King"). Claims 14-16 depend from claim 1. King is cited for teaching a semiconductor assembly comprising a chip carrier having a floor and a frame that extends beyond the edges of the frame to form flanges. (See, Office Action, page 7.) Further, King is cited for the teaching that the flanges fit into grooves of a

motherboard or other application. The Office Action stated that one of ordinary skill in the art would know that other applications would include stacked chip modules.

However, King describes and depicts a semiconductor assembly having only a single flange. (See, e.g., King, Figures 5, 6, and 7.) "Pressure plate 30 covers all but one edge of base plate 36, leaving edge conductors 34 formed on base plate 36 exposed for interconnection to an associated circuit board or conventional connector" (emphasis added). (See King, column 5, lines 29-33.) Such an assembly would not fit into a slotted file in such a manner as to allow platelets to be stacked to form a three-dimensional integrated circuit package.

Further, King teaches away from stacking platelets to form a three-dimensional integrated circuit package. King's invention "arose from efforts to redesign single in-line memory modules." (King, column 1, lines 31-32.) King describes that a "row of dies 31 containing desired memory circuit components can be arranged individually within complementary recesses 37 formed across one engagement surface of pressure plate 30." (See King, column 5, lines 33-36.) Thus, King describes arranging memory components horizontally, not vertically.

The combination of Distefano and King does not show or suggest each and every element of Applicants' claimed invention. Accordingly, Applicants submit that claims 14-16 are not obvious in light of the combination of Distefano and King for at least the reasons set forth above.

In light of the above, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103(a).

CONCLUSION

In light of the above amendments and remarks, Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. The Examiner is requested to contact Applicants' representative below if any questions arise or she may be of assistance to the Examiner.

Respectfully submitted,

Dated: August 20, 2004

Lisa M. Schoedel
Reg. No. 53,546
McDonnell Boehnen Hulbert & Berghoff LLP
300 South Wacker Drive
Chicago, Illinois 60606-6709
312 935 2362
schoedel@mbhb.com